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Symmetric Universal Format Conversion Mechanism With Gray Code

ABSTRACT OF THE DISCLOSURE

According to the invention, an ATM cell format extender or converter includes a memory and write and read state machines which are symmetric as facilitated by the memory and signals applied to the state machines. The write state machine receives information defining the format of an incoming ATM cell, and, in response, sequences through a first selected state sequence. While in each state of the selected sequence, the write state machine decodes a particular address in memory in which an associated byte of the incoming cell is stored. The read state machine receives information defining the format of an outgoing ATM cell, and, in response, sequences through a second selected state sequence. While in each state of the selected sequence, the read state machine decodes a particular address in the memory from which an associated byte of the outgoing cell is retrieved, thereby to construct the outgoing cell. The read and write state machines are preferably identical. Each of the write and read state machines in a specific embodiment is a 4-bit state machine with 16 Gray encoded states.

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